THE OPERATION AND USE OF A FAST INTEGRATED CIRCUIT COMPARATOR*

by R.J. Widlar

I. INTRODUCTION

A differential voltage comparator is a high-gain differential input, single-ended output amplifier. The function of the device is to compare a signal voltage on one input with a reference voltage on the other and produce a digital one or zero at the output when one input is higher than the other.

A comparator is useful as a low hysteresis, variable-threshold Schmitt trigger, a pulse-height discriminator, a voltage comparator in A/D converters, a zero-crossing detector, a threshold detector, an oscillator, a high noise-immunity digital line receiver, or in pulse-width modulator applications. A dual comparator, which will also be discussed, can be used as a core memory sense amplifier, a window discriminator in pulse-height analyzers, or a double-ended limit detector for automatic go/no-go test equipment.

This paper will describe the design and application of the μA710 high-speed differential comparator and the μA711 dual comparator. Additional information on the use of the μA711 as a core memory sense amplifier is available in Ref. 1.

II. CIRCUIT DESCRIPTION

A comparator is similar to a differential-input operational amplifier. In fact, operational amplifiers are frequently used as comparators. However, in many applications, the comparator is expected to recover rapidly from saturation, which is its normal operating state. Additionally, the large output voltage swing desired for operational amplifiers is often a disadvantage when the comparator is used to drive low-level logic circuits. The comparator described is designed to overcome the limitations of operational amplifiers in this application. It features extremely fast recovery from saturation and an output which is compatible with practically all integrated logic forms.

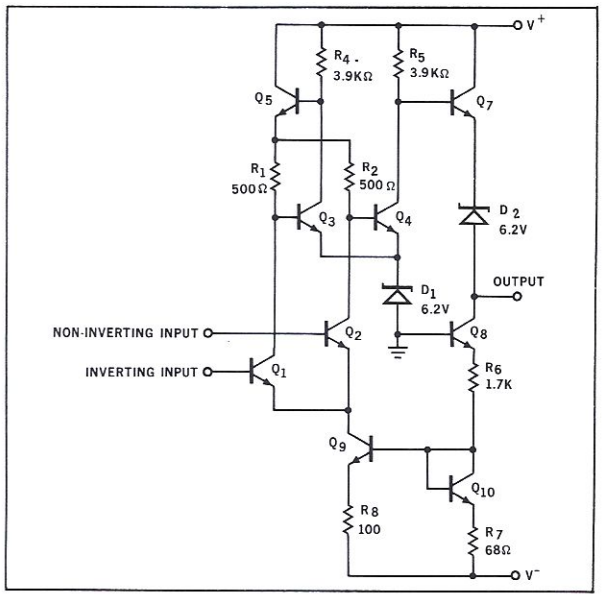

FIG. 1. Simplified schematic.

The operation of the comparator can be explained using the simplified schematic in Fig. 1. A differential input stage (Q_1 and Q_2) is used for low offset. The emitters of the input stage are supplied from a current source (Q_9) to make their collector current insensitive to the common mode input voltage. A balanced second stage is also used: Q_4 is the actual second stage amplifier, while Q_3 provides balanced biasing for Q_4. The second stage can be understood by considering that Q_3 and Q_4 are identical transistors. Their bases are fed from a common voltage point, the emitter of Q_5, which

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keeps the input stage collector current out of R_4, through identical resistors (R_1 and R_2). When the input-stage collector currents are equal, the collector currents of Q_3 and Q_4 will be equal, so the second stage is balanced. Q_3 also functions as a unity-gain amplifier that inverts the output of Q_1 and combines it with the output of Q_2 at the base of Q_4. A single-ended output is obtained at the collector of Q_4. One feature of the second stage is that under balanced conditions, the single-ended output is insensitive to changes in positive supply voltage. If the positive supply voltage is increased, the collector currents of both Q_3 and Q_4 will increase such that the voltage on the collector of Q_4 remains constant.

An emitter follower is used at the output of Q_4 to give a high output-current capability. A zener diode (D_1) in the emitters of the second-stage transistors provides a large input-voltage range (the positive input-voltage limit is essentially equal to the voltage on the base of the second-stage transistors). An identical zener diode in the output emitter-follower (D_2) level shifts the output back to a level compatible with logic circuits. Q_8 isolates the output from the diode-compensated bias divider for the input-stage current source. Using the diode-connected transistor, Q_{10}, to compensate for the emitter-base voltage of Q_9 permits the current source to operate with a small voltage drop across its emitter resistor, R_8. This gives an increased negative input-voltage limit.

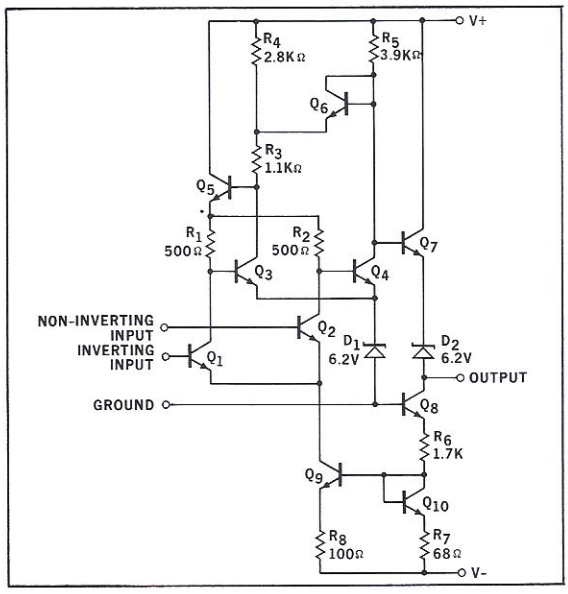


FIG. 2. Schematic diagram of the μA710.

The complete schematic of the μA710 in Fig. 2 shows the addition of Q_6 connected as a diode. This limits the positive output swing both to increase speed and to give compatibility with certain integrated logic families.

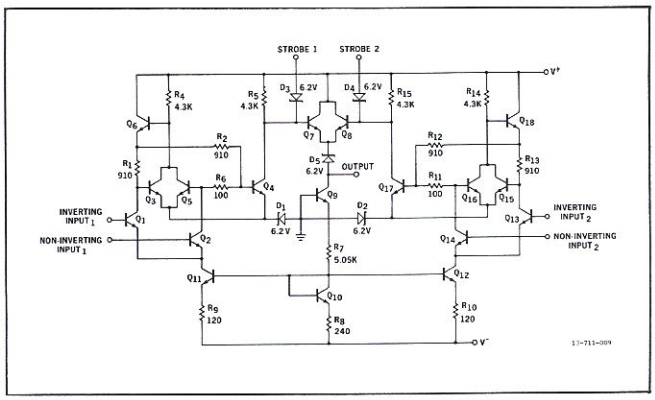


FIG. 3. Schematic diagram of the μA711.

A schematic diagram of the μA711 dual comparator is shown in Fig. 3. The outputs of two individual comparators are OR'ed at the emitter followers. Only a single level-shifting zener diode and bias divider are used. Zener diodes on the bases of the output emitter followers provide a method of disabling the individual channels: when the strobe terminal on one side is held down to ground level, the output of that side cannot rise. The strobe terminal can also be used to clamp the positive output swing, because the output voltage will always be at least one diode drop less than the voltage on the strobe terminal; hence, no clamping diode is used. The output sink-current capability of the μA711 is less than that of the μA710, both to reduce power dissipation and to allow a large number of μA711's to be wire OR'ed at the output.

Another difference between the μA710 and μA711 is that a transistor has been added in the second stage. This transistor (Q_5) reduces the base drive on Q_4 when it saturates to give lower power dissipation and reduced storage time. When the comparator is operating in the active region, the collector current of Q_2 produces a voltage drop across R_6 that cuts off Q_5, so that it does not affect operation. This saturation-limiting scheme is discussed in greater detail in Ref. 1.

The transfer function of a comparator describes its operation in quite general terms. The transfer function of the μA710 is given in Fig. 4 while that of the μA711 is given in Fig. 5.

A mathematical analysis of the comparator operation is given in Appendix A. It is shown that circuit performance is not affected by the loose component tolerances encountered with monolithic construction but depends on how well various parts match—something that is easily done in an integrated circuit. Since this matching can be maintained well over an extremely wide temperature range, the comparator is relatively insensitive to changes in operating temperature.

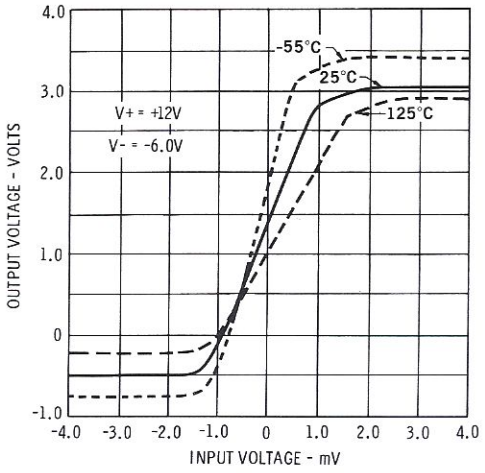


FIG. 4. Voltage transfer characteristic of the μA710 .

In addition, it is demonstrated in the Appendix A that the comparator is not greatly affected by supply voltage variations over a wide range. The only significant parameter variation is voltage gain, but this is reduced to a second-order term in normal applications.

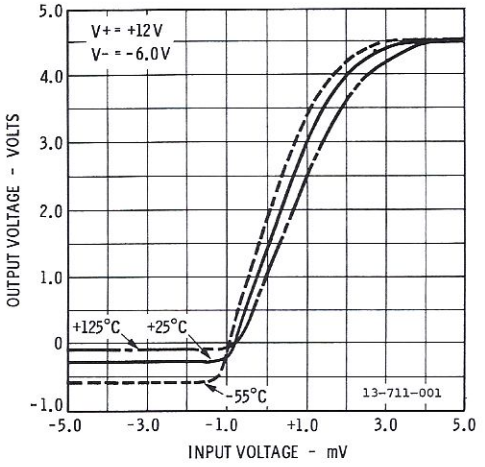


FIG. 5. Voltage transfer characteristic of the μA711 .

III. SPECIFICATION METHOD

The function of a comparator is to produce one digital state at its output when the input signal is above a reference voltage and the opposite digital state when the input is below the reference. The questions to be answered by a set of specifications, in addition to the usual ones of supply voltage, power dissipation and absolute maximum ratings, are (1) the accuracy with which the comparator can distinguish between the input signal and the reference signal and the effect of source resistance on accuracy; (2) how rapidly the comparator can make this distinction and what influence the speed of a decision has on accuracy; and (3) the ability of the comparator to drive different types of logic loads.

DC Accuracy

The first question can be disposed of by defining an input offset voltage as the voltage between the comparator input terminals when the output is just at the threshold voltage of the logic. When the output is at the logic threshold voltage, a very small change in input voltage will cause the output of the logic circuit to swing from zero to a one state. It is not necessary for the comparator output itself to swing from the zero to one state as this does not provide any additional logic output, only more noise immunity. As a matter of fact, when the offset is defined in this manner, the gain of the logic circuit can be added to the gain of the comparator in determining overall gain accuracy. This gives, for example, an equivalent gain of 50,000 when the μA 710 is operated with Fairchild DTL. This combined gain is high enough, with practically all logic circuits, that the voltage gain does not usually need to be considered in determining DC accuracy—the offset voltage alone is enough.

The effect of nonzero source resistances on the accuracy can be taken into account using the input offset current, when the DC resistances seen by the two input terminals are equal, or the input bias current, when the input resistances are very much different. To prevent the necessity of using worst-case values of offset voltage and offset current, the offset voltage can also be specified for the case where the resistances on each input are equal to or less than a given amount. The use of input resistance to determine loading is not valid with a comparator. The input impedance varies rapidly as the differential input voltage goes through zero and is in excess of a megohm for input voltages greater than a couple hundred millivolts.

Response Time

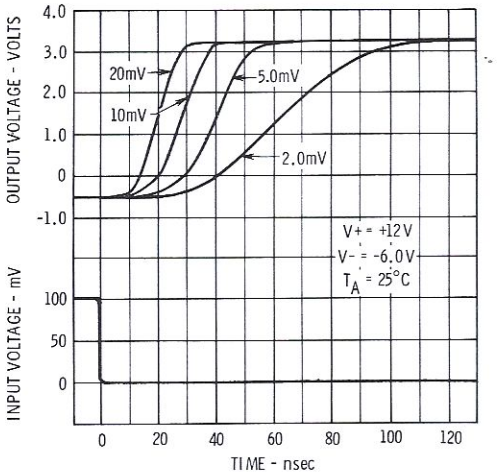
The second question is a little more difficult. The response time could be defined in many ways. A worst-case situation would be where the comparator is used to determine the height of a large pulse. For example, the situation where a DC reference signal (say 0.1 volt) is applied to one comparator input and a step function is applied to the other can be considered.

Before the step function is applied, the comparator is completely saturated in one direction by the reference voltage (the comparator will actually reach complete saturation with less than 100 mV across the input terminals). Some time after the step function arrives, the comparator output will reach the logic threshold voltage if the step height differs from the reference voltage only by the offset voltage. However, this length of time, in the absence of overshoot, would supposedly be infinite, or at least difficult to determine. Therefore, the response time must be measured with some overdrive in order to have any real meaning. That is, the

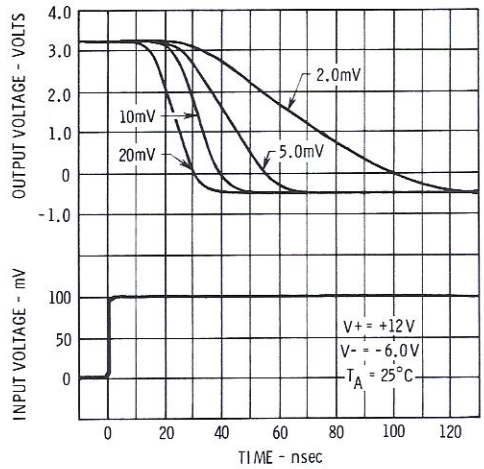
input step height must be increased by some amount over that required to just barely bring the output from saturation to the logic threshold voltage. The response time can then be defined as the interval between the application of the input step and the time when the output crosses the logic threshold voltage. The error encountered in making the decision within this period of time is then the amount of overdrive required.

This response time will be relatively independent of the step height and reference voltage as long as they are in excess of 100 mV. Smaller step heights will give faster response times since the comparator will not be thoroughly saturated.

Figure 6a gives the response time of the μA710 for a 100 mV input step and overdrives of 2, 5, 10, and 20 mV with a positive-going output. Figure 6b does the same for a negative-going output.



a. positive-going output.



b. negative-going output.

FIG. 6. Response time of the μA710.

With the comparator design described, the response time for a positive-going output is most indicative of performance because it depends on the delay time of the input stage, the storage time of the second stage, as well as the feedback and output capacitances of the second stage. For a negative-going output, the storage time of the second stage is eliminated; additionally, the second-stage transistor is able to discharge its output capacitance faster than the collector load resistor can charge it. Therefore, the response time for a negative-going output will always be faster than that for a positive output, in the absence of capacitive loading, so only the latter actually needs to be specified.

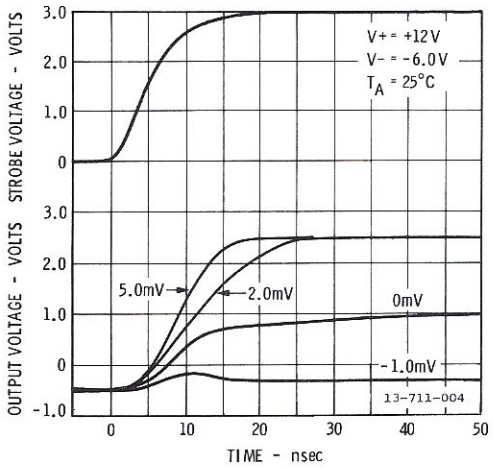


FIG. 7. Strobe release time of the μA711 for various input signals.

With the μA711, the speed of the strobe circuitry is also important. A strobe release time can be defined as the time required for the output to rise to the logic threshold voltage after a positive step function has been applied to the strobe terminal (the strobe signal does not actually have to be a step function as long as it is faster than the measured strobe release time). A DC input signal that will give a positive output when the strobe is released is assumed with this definition. When the strobe voltage returns to zero, it will drop the voltage on the base of the output emitter follower at a speed which is limited only by the fall time of the strobe voltage. Therefore, the strobe fall time is not pertinent.

The strobe release time of the μA711 is shown for various input conditions in Fig. 7. The 0 mV curve is for an input condition that would put the output at the logic threshold voltage under DC conditions. The curve below that is for 1 mV less input voltage and gives an indication of the feed-through of the strobe pulse when the comparator is barely turned off (it is necessary to wire the comparator into the circuit minimizing the stray capacitance between the strobe terminal and the inputs in order to keep this feed-through small). The 2 mV and 5 mV curves represent actual operating conditions and give strobe release times of 14 ns and 10 ns, respectively. In these curves, the output does not rise to the maximum output level because of the clamping action

of the strobe circuitry when a low-amplitude strobe pulse is used. The test conditions shown are representative of the case where the comparator is used with Fairchild RTL.

Logic Compatibility

Specification of logic compatibility can be approached by ensuring that the comparator can drive the logic into full saturation under worst-case conditions. After this is done, it is only necessary to take into account the difference between the threshold voltage of the logic used and the logic threshold specified for the comparator to determine the influence on offset voltage. The effect of differing logic threshold voltages on offset is less than a millivolt with most standard logic circuits so even this can be neglected in the majority of applications.

In general, performance is guaranteed by specification of positive and negative output levels, with and without load, which are compatible with the logic used. The following information is useful in establishing the limitations of the comparator, the circuitry to be used, and the operating conditions under which the comparator is to be specified.

When operated with standard resistor-transistor logic (Fairchild Micrologic® integrated circuits), the comparator is roughly equivalent to a buffer element and can drive a large fan-out. However, since the comparator operates from a higher supply voltage than a buffer, the internal dissipation with a one-level output can become excessive. In addition, the large output current available from the comparator can overdrive the logic and cause excessive storage. For these reasons, it is advisable to insert a resistor in series with the output of the comparator to limit the current. Recommended values with both the μA 710 and μA 711 are 1.5 KΩ for a fan-out of one, 510 Ω for a fan-out of two, and 270 Ω for a fan-out of three. A small (100 pF) capacitor can be connected in parallel with this resistor to increase the speed of the logic.

Essentially the same rules apply for low power resistor-transistor logic (Fairchild MWμL). Recommended values of series resistance are 4.7 KΩ for a fan-out of one, 2.2 KΩ for a fan-out of two, and 1.3 KΩ for a fan-out of three. Again, a small capacitance can be added across the resistor for increased speed.

The limiting factor when operating with diode-transistor logic (Fairchild DTμL) is the ability of the comparator to supply the required sink current. The μA 710 can drive a DTμL fan-out of one, but an external 3.6 KΩ resistor must be added between the output and the -6 V supply for a fan-out of two, and a 2.2 KΩ resistor must be used for a fan-out of three. With the μA 711, at least four devices must be OR'ed before they can provide enough sink current for a DTμL fan-out of one. If a single comparator is used to drive a DTμL circuit, a 5.6 KΩ resistor must be inserted between the output terminal and the -6 V supply for a worst-case fan-out of one. For a fan-out of two, a 2.4 KΩ resistor must be used.

With transistor-transistor logic (Fairchild $T^2\mu$L) the same rules regarding sink current used with DTμL must be followed. The high-level, reverse current encountered with $T^2\mu$L can be disregarded because both the μA 710 and μA 711 are able to supply considerable current in this direction and because the permissible fan-out is low, being restricted by the available sink current.

Both the μA 710 and the μA 711 can be used to drive complementary-transistor logic (Fairchild CTμL) directly. The fan-out, however, is limited to one, or perhaps two, by the ability of the comparator to supply the required current at the output high level.

The one remaining point to be covered on logic compatibility is the strobe of the μA 711. In the low state, it is necessary to sink 1.2 mA, typically, at the strobe terminal to hold one side of the comparator off. This current is only required if the side being held off is turned on internally. Hence if the comparator is used in an application where only one side can be on at a time, it is only necessary to provide sink current for one strobe—otherwise it is required to sink 2.4 mA to hold both sides off. In the high state, the strobe does not load the logic appreciably. The high level required to release the strobe depends on the type of logic used in that the output of the comparator will be clamped to a voltage that is one diode drop less than the strobe voltage.

It is not advisable to leave the strobe terminal floating, particularly in high-speed circuits, because of stray capacitance effects. The strobe terminal should be connected to the logic supply voltage (or any other voltage less than +6 V) if it is not being used.

IV. APPLICATIONS

The basic circuit for using the comparator is shown in Fig. 8. A reference voltage between $\pm$ 5 V is inserted on one input and the signal is inserted on the other. When the input exceeds the reference voltage, the output switches either positive or negative depending on how the inputs are connected. The circuit has a variety of uses. It can be employed as a voltage comparator in A/D converters, where one input is driven by the analog input signal and the other by a ladder network. It also has use as a tape or drum memory sense amplifier and threshold detector. Other applications are a high noise immunity buffer for going from high level logic into low level integrated circuits or a pulse-shape restorer in digital circuits.

General Hints

In order to achieve maximum accuracy in the circuit of Fig. 8, the DC resistance of the signal source (R_S) should equal the source resistance of the reference voltage (R_1). When this is done the bias currents of the two inputs produce nearly equal drops across these source resistances; and the increase in offset is due only to the offset current, which is usually more than an order of magnitude less than the bias current. These resistances should also be made as low as possible, preferably less than 200 Ω for best performance.

Although the input voltage range of the μA 710 and μA 711 is ± 5 V, the maximum voltage between the inputs is also ± 5 V. If one of the inputs is at + 5 V, for example, the other can only be driven as low as ground potential without exceeding the differential input voltage limit. It is important to observe this maximum rating since exceeding the differential input voltage limit and drawing excessive current in breaking down the emitter-base junctions of the input transistors could cause gross degradation in the input offset current and input bias current.

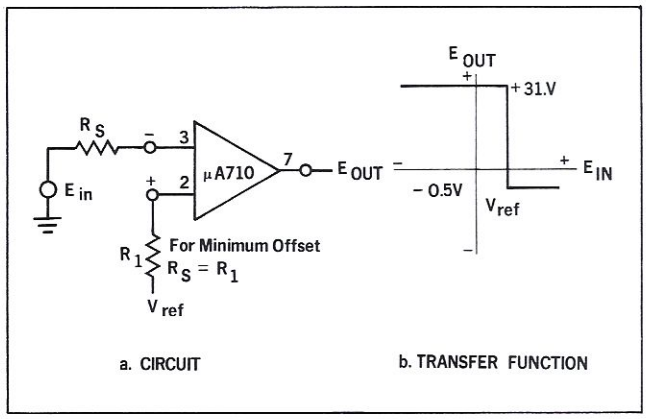


FIG. 8. Basic level detector circuit.

Exceeding the absolute maximum, positive input voltage limit of the device (+ 7 V) will saturate the input transistor and can cause damage through excessive current. However, even if the current is limited to a reasonable value so that the device is not damaged, erratic operation can result. For example, when the transistor on the inverting input saturates, it no longer functions as an inverting amplifier stage; instead, it makes a direct connection between the input and the base of the second-stage transistor, so the inverting input becomes a non-inverting input. A similar situation exists for the non-inverting input. The negative limit of the input voltage range is specified at -5 V, but it is necessary to increase the negative supply voltage to -7 V to ensure that the input stage current source does not saturate at -55°C, causing improper operation.

Some attention to power supply bypassing is required with both the μA 710 and μA 711. These devices are multistage amplifiers with gain to several hundred megacycles. Long, unbypassed supply leads or sloppy layouts can therefore cause oscillation problems. Bypassing with electrolytic or tubular paper capacitors is ineffective. What is recommended is that both the positive and negative supplies be bypassed to ground using low-inductance, disc-ceramic capacitors (0.01 μF) located as close as practical to the device. A neat physical layout, keeping the input away from the output, is also important. The strobe of the μA 711 should also be kept away from the inputs if fast-rise strobe pulses are used. The strobe terminal, if unused, should not be left floating in high-speed circuits because of stray capacitive effects.

One side of a μA 711 can be used in much the same manner as a μA 710. However, the inputs of the unused side should be grounded so that the input current source transistor on that side does not saturate and disrupt the bias divider. It is also advisable to ground the strobe terminal to prevent interaction between the unused side and the active side.

In some applications where there are large amounts of noise on the signal when it is passing through the threshold of a level detector, it is desirable to have some hysteresis in the transfer characteristic. The hysteresis is generally made somewhat greater than the maximum expected noise. A circuit using external positive feedback to produce hysteresis is shown in Fig. 9.

The upper and lower trip points of this circuit can be written as follows:

$$V_{UT} = V_{ref} + \frac{R_1\left[V_{O(max)} - V_{ref}\right]}{R_1 + R_2} \qquad (1)$$

and

$$V_{LT} = V_{ref} + \frac{R_1\left[V_{O(min)} - V_{ref}\right]}{R_1 + R_2} \qquad (2)$$

Therefore, the hysteresis is

$$V_H = V_{UT} - V_{LT}$$

$$= \frac{R_1\left[V_{O(max)} - V_{O(min)}\right]}{R_1 + R_2} \qquad (3)$$

The minimum amount of hysteresis obtainable is determined by the forward gain and output swing of the comparator. It should not be made less than about 5 mV or oscillation will occur on the positive portion of the transfer function

if the small signal gain of the comparator is not greater than the ratio of the feedback resistors. Reduced hysteresis can usually be obtained when the comparator is used with logic circuits by taking the positive feedback from the output of the logic. The additional gain of the logic permits a smaller hysteresis. For example, with the additional gain of a DTμL gate, it can be made less than 0.2 mV.

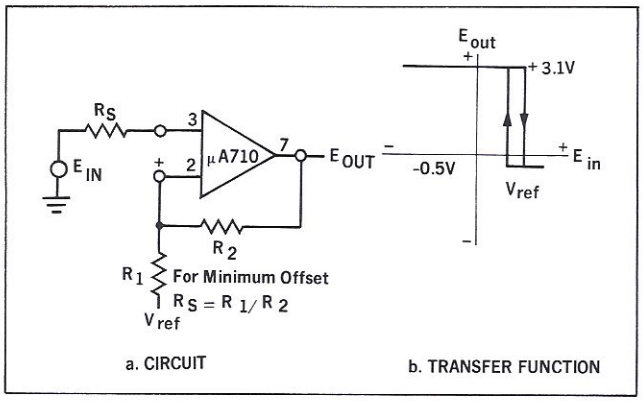


FIG. 9. Level detector with hysteresis .

With the connection in Fig. 9, the μA710 can be substituted for a Schmitt trigger. It has the advantage, though, that nonzero trip points can be obtained and both the upper and lower trip points are easily and independently adjustable over a wide range of positive and negative voltages.

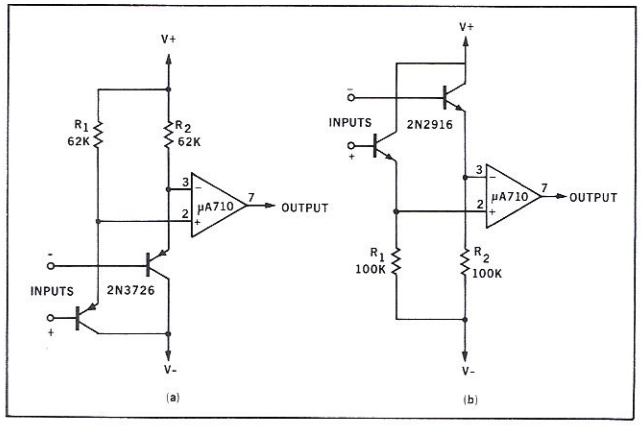


FIG. 10. Circuits for obtaining a higher input resistance .

In a number of applications the input currents of the μA710 and μA711 are high enough to cause significant error due to loading of the signal and reference-voltage sources. In these instances, a transistor pair can be used in front of the comparator to reduce the input currents. Two possible circuits are given in Fig. 10. The circuit using the PNP pair is most flexible in that the full input voltage range of ±5 V is still available. The NPN circuit is quite satisfactory when the comparison is made at input voltages above -2 V. It is possible to balance out the comparator offsets in these circuits by unbalancing the emitter resistors (R_1 and R_2) on the input transistors.

The speed of the comparator is affected somewhat by the addition of the input stage. This is caused primarily by collector-base capacitance of the input transistors loading the source. The transistors shown in Fig. 10 were selected for a low collector-base capacitance as well as a high current gain, and should load the source with a total capacitance less than 10 pF.

Line Receivers

Frequently in the design of digital systems it is necessary to interconnect various equipment over long lines where the possibility of picking up considerable noise exists. In these cases it is desirable to use a line receiver that has considerably more noise immunity than standard logic circuits

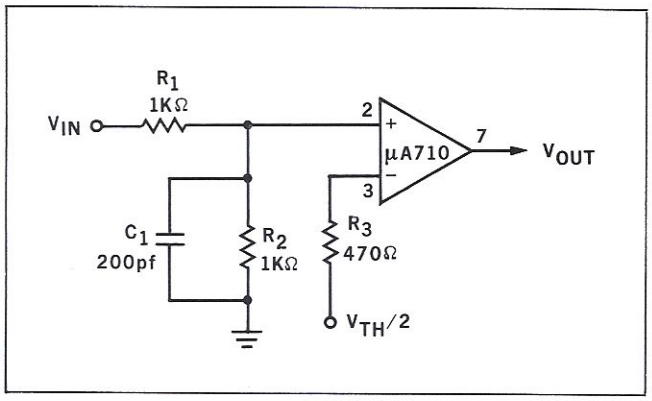


FIG. 11. High noise-immunity line receiver for slow, high-level logic .

to precondition the logic signals. Figure 11 shows a line receiver using a μA710. The resistive divider on the input of the comparator permits higher level logic signals than are possible with the μA710 alone (up to ±14 V in this case). It is also possible to put a capacitor at the comparator input (C_1) to make the circuit insensitive to fast noise spikes. Because of the high gain of the comparator, fast-rise output pulses can be obtained even with this integrating capacitor.

It is sometimes necessary to design a piece of logic equipment to interface with any one of the many types of digital logic (RTL, DTL, CML, CTL, etc.). These types can have widely different logic levels so the input circuitry must possess considerable flexibility to accommodate all. A circuit that satisfies the requirements is shown in Fig. 12. The input threshold voltage can be adjusted over a ±5 V range with a single control. A μA702A operational amplifier provides an adjustable reference voltage with a very low source imped-

ance. A single amplifier can handle over a hundred comparators.

Double-Ended Limit Detectors

In the design of test equipment, a circuit which will indicate when a voltage goes outside some preset tolerance

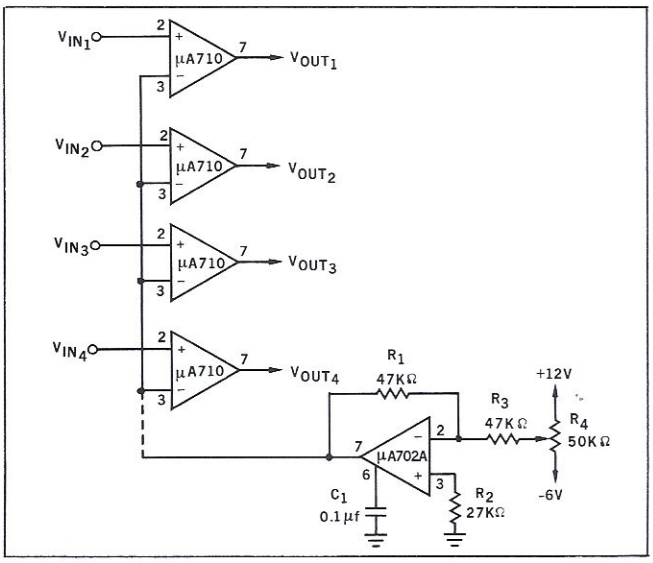


FIG. 12. Adjustable-threshold, high-noise-immunity line receivers.

limits is frequently called for. The circuit in Fig. 13, using a μA711 dual comparator, will accomplish this function. A lower limit voltage (V_{LT}) and an upper limit voltage (V_{UT}) are supplied to the dual comparator. When the input voltage exceeds the upper limit or drops below the lower limit, the output of the comparator swings positive and turns on the lamp driver. A feature of the circuit is that the limit detector can be disabled when it is not being used by grounding

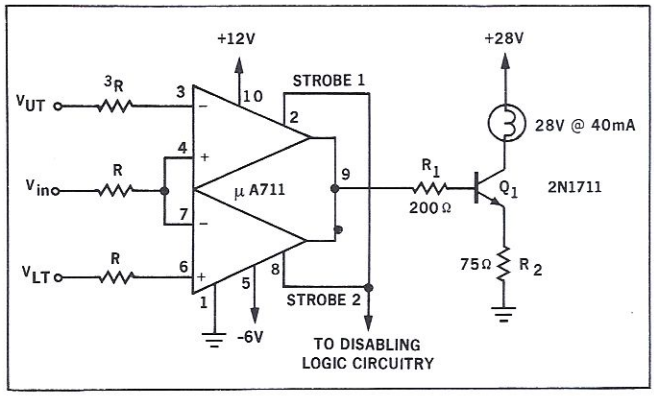


FIG. 13. Double-ended limit detector for automatic go/no-go test equipment.

the strobe terminals. In addition, up to eight dual comparators can be wired with common outputs and be used to feed a single lamp driver.

The peak output current of the lamp driver is limited while the bulb is turning on and the filament resistance is low by R_2. R_1 limits the output current of the comparator after the lamp driver saturates. The relative values of the source resistances for the signal and reference voltages should be as indicated on the schematic to make the accuracy dependent on offset currents rather than bias currents. These resistances should also be as low as possible.

A similar level detector circuit* is shown in Fig. 14. In this circuit hysteresis is provided at both the upper and lower threshold levels. A μA709 operational amplifier serves as both a buffer and a difference amplifier. With the component values shown, an output is obtained from the μA711 when the difference between the two input voltages exceeds 0.55 V. A hysteresis of approximately 50 mV is obtained.

Even more complex level-sensing circuits are possible. A typical example of where they might be used is test equipment for grading zener diodes by voltage. The voltage output of the zener being tested could be fed to a number of

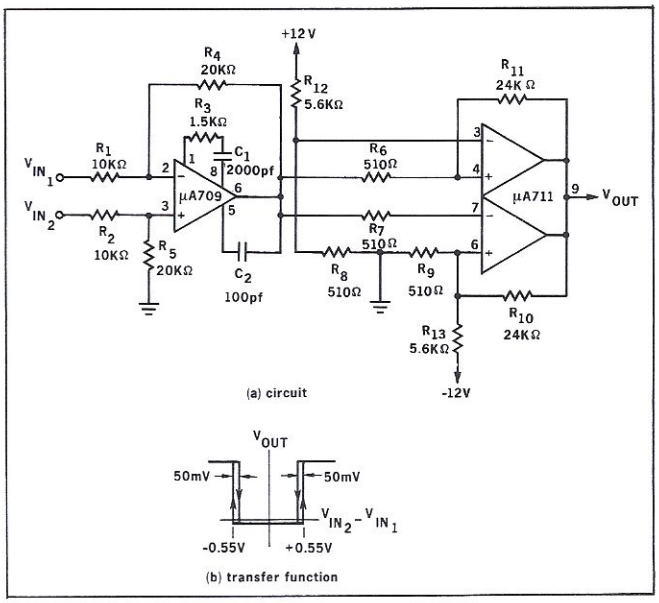


FIG. 14. Double-ended differential threshold detector with hysteresis.

μA710's. Each of these comparators would sense one of the grade-separation voltages, and the outputs would be fed to logic which would drive the readout circuits. Alternately, a μA711 could be used for each one of the voltage brackets, thereby eliminating the logic.

*Suggested by Frank Thomas, Bendix Corporation, Eclipse-Pioneer Division.

Multivibrators

It is possible to use the μA710 as a one-shot multivibrator with the circuit shown in Fig. 15. It has the particular advantage that the trigger point can be determined within ±10 mV over a ±5 V range. The trigger level of the one-shot is equal to the externally set threshold voltage (V_{ref}). The duration of the output pulse is given by

$$t = (R_2 + R_3)\, C_1 \log_e \left[\frac{\Delta V_O\, R_2}{V_{ref}(R_2 + R_3)} \right] \qquad (4)$$

where ΔV_O is the difference between the positive output level and the negative output level.

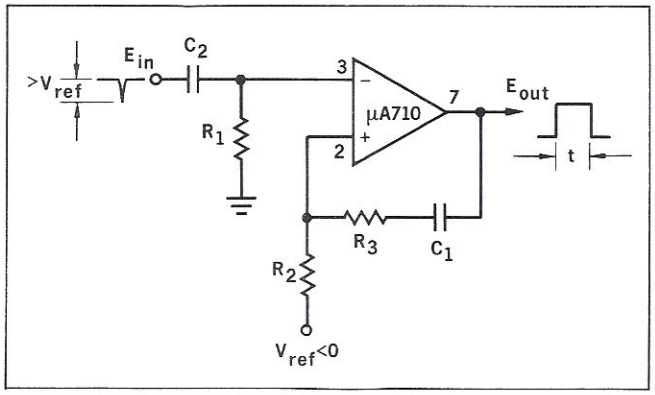


FIG. 15. One-shot multivibrator.

The circuit in Fig. 15 gives a positive output pulse for a negative trigger with $V_{ref} < 0$. For $V_{ref} > 0$, a negative output pulse for a positive trigger is realized. Positive outputs for positive trigger and negative outputs for negative trigger can also be obtained by connecting the input differentiating capacitor to the non-inverting input. However, the interaction between the trigger and feedback circuitry must be taken into account.

A free-running multivibrator using the μA710 is illustrated in Fig. 16. A large amount of DC negative feedback, along with a resistor connected to the negative supply, is used to set the output of the μA710 in the center of its active region to ensure starting and reasonable symmetry in the output waveform. The capacitor reduces the negative feedback at high frequencies giving net positive feedback and oscillation.

The relative resistance values for the multivibrator are computed to give a DC output voltage in the center of the active region of the μA710, assuming that C is removed and the comparator is treated as an operational amplifier. With the relative values given in Fig. 16, the period of oscillation is

$$T = 1.8\,RC \log_e \left[\frac{V_{O(min)} - V_{O(max)}}{0.1\,V^- + 0.45\,V_{O(min)}} \right] \qquad (5)$$

where the sign of V^- and $V_{O(min)}$ must be observed. Using typical values, Eq. (5) becomes

$$T = 2.7\,RC \qquad (6)$$

There are certain restrictions on the range of R in Fig. 16. If R is made smaller than about 1 KΩ, the output sink current of the μA710 may not be large enough to swing the output all the way negative. On the other hand, if R is made larger than about 24 KΩ, the input offset current could seriously degrade the symmetry of the output waveform and could possibly give start-up problems.

Because of the fast response of the μA710, the multivibrator circuit can be operated to quite high frequencies. It has been used successfully to frequencies as high as 5 MHz. At high frequencies, performance can be improved somewhat by connecting a small capacitor between the output and the non-inverting input.

Switching Regulator

Another circuit which demonstrates the flexibility of the μA710 is the high-power switching regulator shown in Fig. 18. It is capable of delivering an output current greater than 2 A at better than 85-percent efficiency. The output voltage is adjustable over a very wide range, and the load and line regulation is better than 0.5 percent. The operating frequency is about 10 kHz and the output ripple is less than 10 mV. Current limiting, which keeps the dissipation in the power-switch transistor at a safe value, is provided.

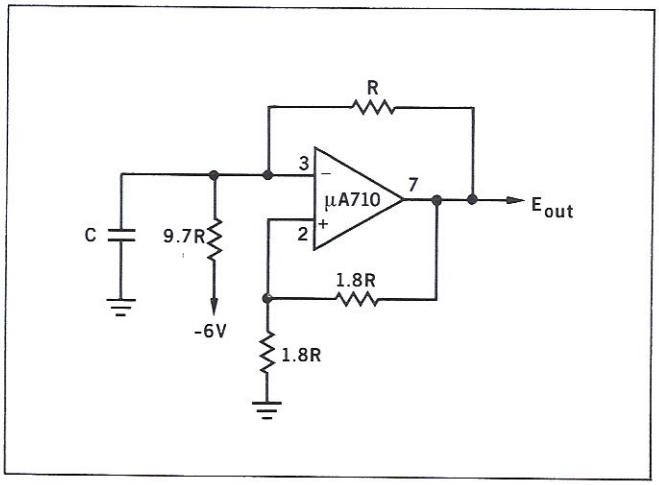


FIG. 16. Free-running multivibrator.

The basic circuit can be explained with the aid of the simplified schematic given in Fig. 17. The μA710 is connected as a level detector with hysteresis, and the regulator reference voltage is fed to the non-inverting input. Therefore, the comparator will switch on when the voltage on the inverting input is slightly below the reference; and it will switch off when this voltage is slightly above the reference. When the comparator turns on, it drives Q_1 which saturates Q_2, applying the DC input voltage to the load through L_1. The output voltage is sent back to the inverting input of the comparator; hence, when the output voltage rises above the reference voltage, the comparator turns off. The output voltage now falls at a rate determined by L_1 and C_1. When it drops by an amount equal to the hysteresis, the comparator turns back on; and the output again rises. Therefore, the circuit operates in a self-oscillating mode in such a way as to main-

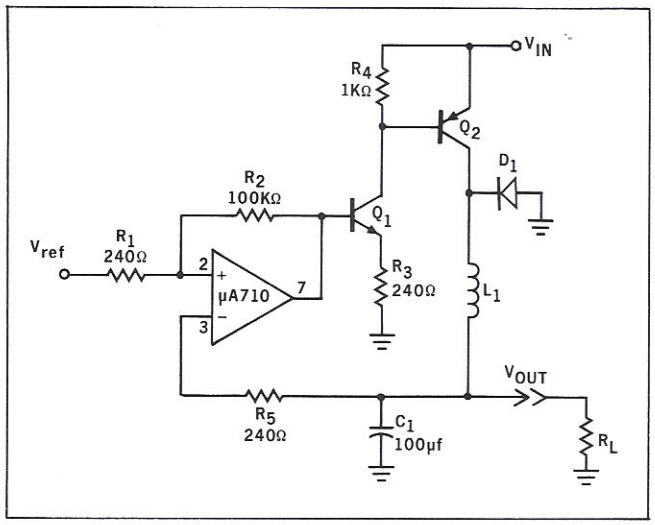


FIG. 17. Simplified schematic of the switching regulator.

tain a constant ripple voltage across the load independent of input voltage or load.

The purpose of the diode in Fig. 17 is to provide a return path for the inductor current after the switching transistor turns off. The size of the inductor has a considerable influence on the efficiency. If the inductor is large enough to maintain a relatively constant current through the switching cycle, it is easy to see how it is supplying the load current continuously. However, this current (which is equal to the load current) is only being supplied by the input voltage source for part of the cycle. The inductor is acting as a source, supplying current through the diode, for the remainder. Therefore, the average input current is less than the output current. As the inductor is made smaller, the peak currents become greater, increasing the losses in the power switch transistor, the inductor, and the diode.

An interesting feature of the circuit is that if the inductor is made large enough so the current through it does not go to zero through the cycle, the operating frequency will be affected little by the load or the input voltage. Instead, it will be determined by the inductor, the output capacitor, and the amount of hysteresis on the comparator.

The complete schematic of the switching regulator is shown in Fig. 18. A pre-regulator (Q_3, R_5, and D_3) is used to supply current for the temperature-compensated, voltage-reference diode, D_1. The pre-regulator also provides power for the μA710. The comparator is operated from supply voltages of 0 V, +6 V, and +18 V instead of the usual positive-negative voltage combination. The +6 V is provided by zener diode, D_2. An emitter-follower transistor, Q_4, is added at the output to increase the output-current capability. Q_3 serves as the current-limiting transistor: when the peak output current exceeds about 3 A, the power switch transistor is no longer required to maintain the output voltage. Instead, Q_3 supplies current directly to the inverting input of the comparator. Therefore, the power transistor still switches and does not have to handle anywhere near the full short-circuit current at the maximum supply voltage as would be required with conventional current-limit schemes.

The output voltage is established with the resistive divider formed by R_7 and R_8. A potentiometer can be substituted to make this voltage continuously variable with the zener reference voltage determining the lower limit of adjustment and the input voltage and breakdown voltage of the discrete transistors determining the upper limit. If additional ripple filtering is desired, it can be added without degrading regulation by connecting R_8 to the output of the added filter instead of to C_6, but keeping C_4 connected to C_6 to provide the self-oscillating feedback. R_8 can also be used for remote-voltage sensing in this manner.

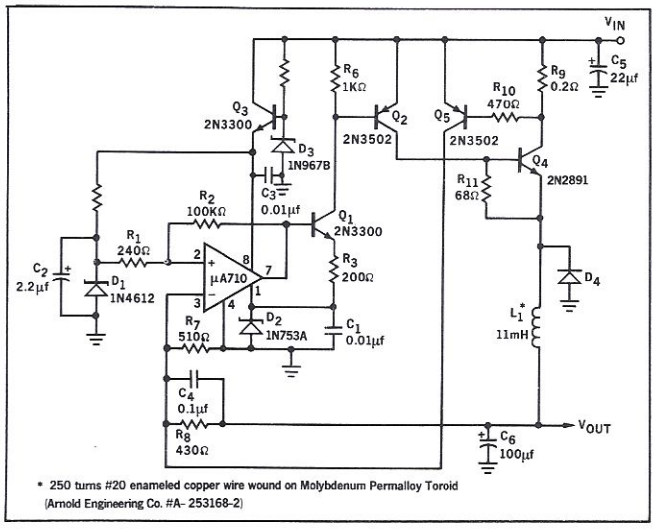


FIG. 18. High-power switching regulator.

Because of the relatively high operating frequency of the circuit, all large value capacitors should be solid tantalum and all the low-value capacitors should be disc ceramic in order to provide adequate bypassing.

Switching Power Amplifier

A pulse-width-modulator/power switch that can be used to drive DC servo motors, proportional-actuators or other loads requiring bi-directional control can also be made with the μA710 or μA711. A circuit is shown in Fig. 20. The principle of operation is similar to that of the switching regulator and can be explained using the simplified schematic in Fig. 19.

The power-switch bridge in Fig. 19 functions such that if Q_2 is turned on, Q_3 is likewise turned on through R_5, applying the full supply voltage across the load in one direction. Alternately, when Q_5 is turned on, Q_4 is also turned on, applying the supply voltage across the load in the opposite direction. Hence, either Q_2 or Q_5 can be switched on and off at a high frequency, with the duty cycle of this switching operation determining the average value of the load voltage. Since the power losses in the transistors are small when they are either saturated or cut off, large amounts of power can be controlled without dissipating much power in the control transistors.

The average value of the load voltage is sensed by a μA709, which is connected as a differential, integrating amplifier. The input signal to the power amplifier (V_{IN}) is also fed to this μA709. The output voltage of the μA709 can be written in terms of these voltages, using standard operational amplifier theory:

$$V_O = V_{IN} - \frac{R_{15}}{R_{17}} V_{OUT} \qquad (7)$$

where it is assumed that $R_{14} = R_{15}$ and $R_{16} = R_{17}$.

The output of the μA709 is fed to two μA710 comparators, which in turn drive a current switch. One comparator (A_2) controls the turn on of one side of the switching bridge Q_2, while the other controls the opposite side. Positive feedback, which provides hysteresis, is used on both comparators.

With a positive input voltage, the output of the μA709 will go positive, turning on one comparator (A_3). This will drive one side of the bridge, applying the full supply voltage across the load. This load voltage is fed to the μA709 in

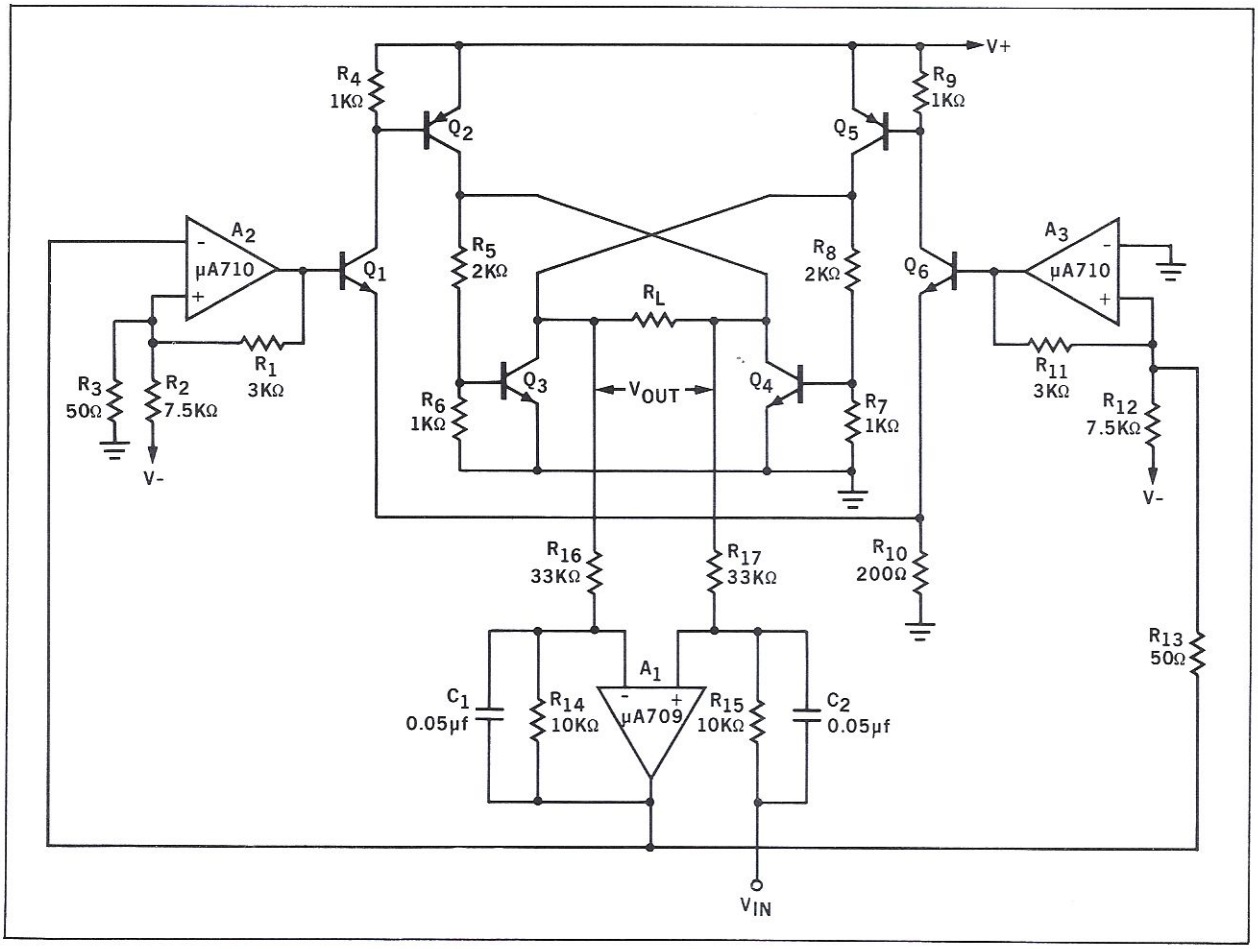


FIG. 19. Simplified schematic of the bi-directional, switching, power amplifier.

such a direction as to make the output swing negative at a rate determined by the integrating capacitors, C_1 and C_2. Power will continue to be applied to the load until the output of the μA 709 falls by an amount equal to the hysteresis of the comparator. The hysteresis is made quite small (50 mV), so the switch will be turned on and off without the output of the μA 709 becoming much different than zero. Hence, Eq. (7) can be set equal to zero, giving

$$V_{OUT} = \frac{R_{17}}{R_{15}} V_{IN} \tag{8}$$

where V_{OUT} is the average value of the output voltage since A_1 integrates the switched waveform across the load.

With negative input signals, operation is identical, except that A_2 is switched on giving an output signal of opposite polarity.

The time required for the integrating feedback amplifier to go from the upper threshold voltage of the comparator where the switch turns on to the lower threshold where the switch turns off depends only on the voltage switched across the load, the input resistance of the amplifier (R_{17} or R_{16}), and the integrating capacitor (C_1 or C_2). The voltage switched across the load is also constant and very nearly equal to the supply voltage (V^+). Therefore, for varying input signals, the on time of the voltage switched across the load will be constant and the frequency will vary to control the power. The on time is given by

$$t = R_{17} C_2 \left(\frac{V_H}{V^+}\right) \tag{9}$$

where V_H is the hysteresis of the comparator given by Eq. (3). The average value of the voltage across the load will be

$$V_{OUT} = V^+ \left(\frac{t}{T}\right) \tag{10}$$

where T is the period of the switched waveform. Hence, the frequency of the pulse-width-modulated output will be

$$f = \frac{V_{OUT}}{t V^+} \tag{11}$$

It is necessary to ensure that the hysteresis loops of the two comparators do not overlap. Otherwise the circuit will operate in a class-A mode alternately switching on one side and then the other for the full duty cycle even when the input voltage is zero.

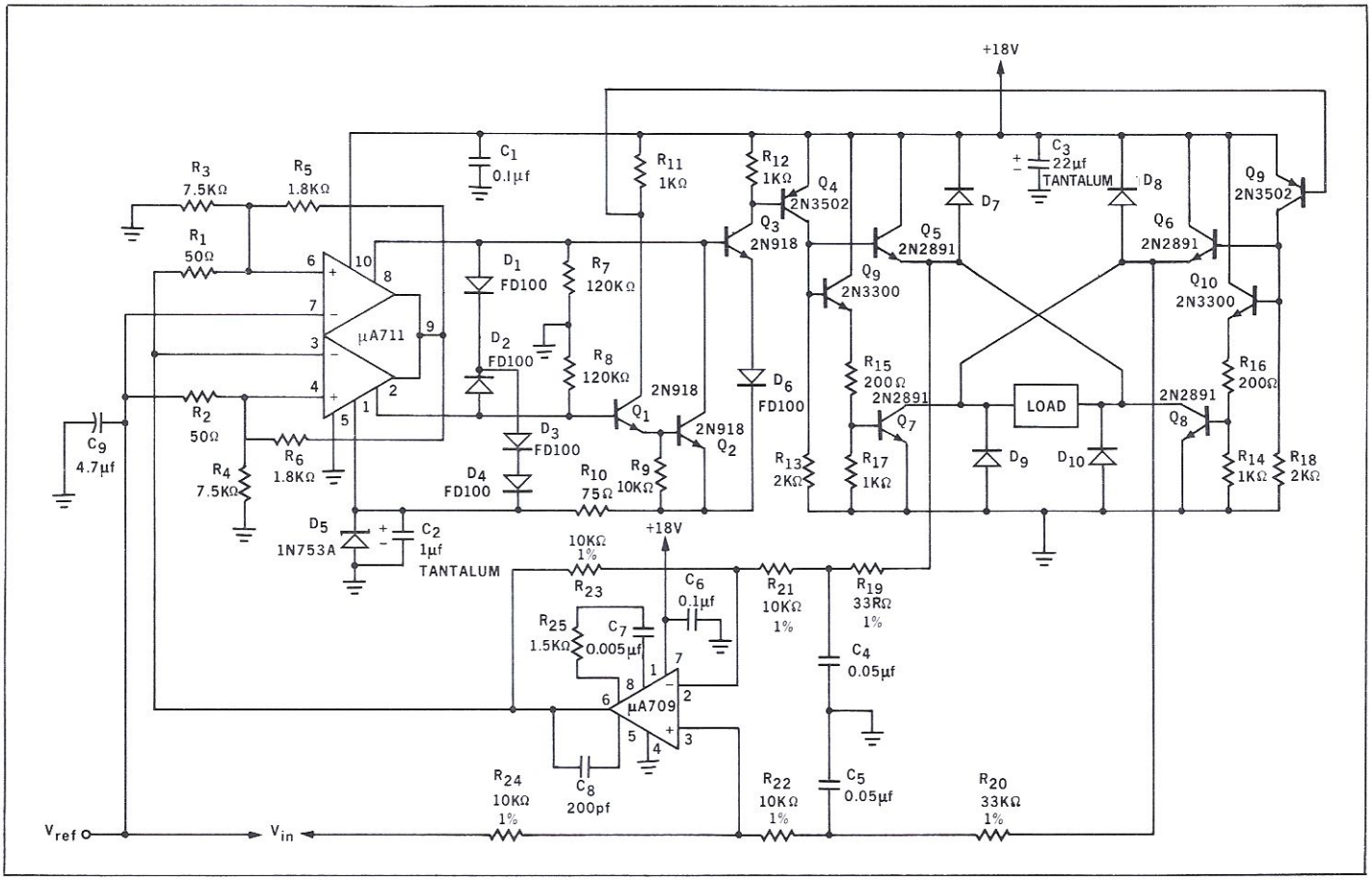


FIG. 20. Complete schematic of the switching power amplifier.

The complete schematic of the power amplifier is given in Fig. 20. In addition to filling in the minor circuit details for the simplified schematic, this circuit operates from a single supply voltage (no negative supply) and provides a much increased power output. Emitter followers (Q_5 and Q_6) have been added to give an output current capability of several amperes. The bases of the bottom transistors in the bridge are driven from separate emitter followers (Q_9 and Q_{10}). This base drive could be obtained from the emitters of Q_5 and Q_6 except that excessive saturation voltage of one of the lower power transistors could cause the other lower transistor to become turned on. Diodes have been included (D_7, D_8, D_9, and D_{10}) to clamp the current spikes obtained with inductive loads.

A μA 711 has been substituted for the two μA 710's. Independent, low-level outputs are obtained by using the strobe terminal as an output terminal (see Fig. 3). Diodes (D_1 through D_4) are used to clamp the voltage being fed to the current switch (Q_1 and Q_3), which drives the power switch. Q_2 and D_6 have been added to ensure that both the positive and negative output channels cannot be driven simultaneously. This is not a problem during operation since the comparator turn-on points are kept separated by R_3 and R_4, but it is necessary to guarantee that both channels cannot be driven when the power is first turned on.

The μA 711 is operated from ground, +6 V, and +18 V while the μA 709 is operated between ground and +18 V. The necessity for a negative supply is eliminated by using a psuedo-ground for the system at some positive voltage that is within the common mode range of the μA 711 and μA 709, which are +11 V and +2 V for the μA 711 and +4 V and +14 V for the μA 709. A convenient value for this voltage is +6 V. The input signal to the amplifier is the voltage difference between the reference and the input terminal.

The location of the integrating capacitors (C_4 and C_5) has been changed to prevent feeding the switching spikes into the input circuitry.

As with the switching regulator, the bypass capacitors should be solid tantalum or disc ceramic to ensure removing the switching spikes.

V. CONCLUSION

Differential voltage comparators which make use of the excellent component matching and low wiring capacitances available with monolithic construction were discussed. The devices have very stable DC characteristics over a wide temperature range and response times superior to discrete-component circuits of comparable performance and power dissipation. Their simplicity and suitability for integration is demonstrated both by the design analysis in Appendix A and by the fact that the μA 710 is constructed on a 35-mil-square silicon die while the μA 711 dual comparator is constructed on a 40-mil-square die—both using the standard Planar-epitaxial process. Photomicrographs of the μA 710 and μA 711 are shown in Figs. 21 and 22, respectively.

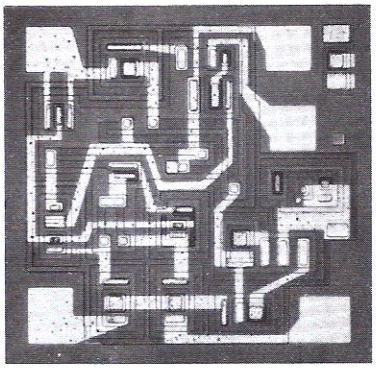


FIG. 21. Photomicrograph of the μA 710 high-speed differential comparator.

General hints intended to acquaint circuit designers with possible peculiarities of these devices were given, and a number of applications were outlined. It has been demonstrated that these microcircuits can be used in a wide variety of applications ranging from simple level detectors, Schmitt triggers and digital line receivers to multivibrators and even pulse-width-modulated regulators and servo-motor drivers. The use of these same circuits in the core-memory field is covered in Ref. 1.

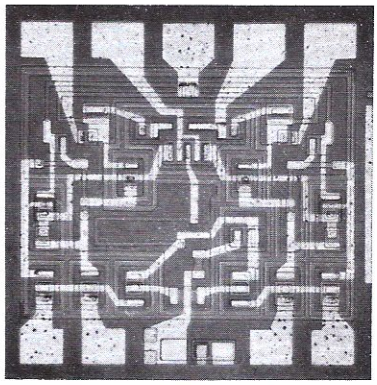


FIG. 22. Photomicrograph of the μA 711 dual comparator.

The parameters necessary to specify the operation of these comparators were defined and explained in the text. Additional information on test methods and test circuits is given in Appendix B.

*Planar is a Fairchild-patented process.

VI. REFERENCES

1. R. J. Widlar, "Core Memory Sense Amplifier Designs Using An Integrated Dual Comparator," Fairchild Semiconductor, APP-123.

2. J. N. Giles, "A Versatile Tester for Linear Integrated Circuits," Fairchild Semiconductor, APP-125.

APPENDIX A

DESIGN ANALYSIS

The purpose of this appendix is to show that the accuracy of the comparator described in the text is primarily dependent on component matching: resistor values, the transistor current gains, emitter-base voltages, zener voltages, and even power-supply voltages may vary over an unusually wide range as long as certain parts are well matched. In the analysis, the simplified schematic in Fig. 1 of the text will be used, since the active region of the comparator, where the refinements of the μA710 and μA711 are inoperative, is under consideration here.

First an expression will be obtained for the output voltage for zero input voltage. It is desired that this be equal to the threshold voltage of the logic circuit that the comparator drives so that the logic state changes as the differential input of the comparator goes through zero. It will be assumed that all the resistors are perfectly matched in ratio, that transistors are perfectly matched, and that the zener diodes are likewise matched, since these are all accomplished over a broad temperature range in an integrated circuit. Further, it will be assumed that the transistor current gains are sufficiently large that the base currents can be neglected (although a more complete analysis will show that the base currents are insignificant if the transistors are reasonably well matched and the current gains are larger than about 10). Finally, it will be assumed in certain places that the emitter-base voltages of all transistors are the same regardless of the collector current both because this can be made true by suitably choosing the transistor geometries and because a factor of two difference in collector current only results in an emitter-base-voltage variation of approximately three percent.

For zero differential-input voltage, the collector currents of the input-stage transistors, Q_1 and Q_2, will be equal since they are identical devices with the same emitter-base voltages. The collector current of the second-stage biasing transistor, Q_3, can be written as

$$I_{C3} = \frac{V^+ - V_Z - \frac{1}{2} I_{C9} - 2V_{BE}}{R_4} \tag{A.1}$$

Similarly, the collector current of the second stage amplifier transistor is

$$I_{C4} = \frac{V^+ - V_Z - V_{BE} - V_{OT}}{R_5} \tag{A.2}$$

where V_{OT} is the output voltage.

For $R_1 = R_2$, these two currents will be equal because of the balanced configuration, so

$$\frac{V^+ - V_Z - \frac{1}{2} I_{C9} R_1 - 2V_{BE}}{R_4} = \frac{V^+ - V_Z - V_{BE} - V_{OT}}{R_5} \tag{A.3}$$

With $R_4 = R_5$, Eq. (A.3) becomes

$$V_{OT} = V_{BE} - \frac{1}{2} I_{C9} R_1 \tag{A.4}$$

It is now necessary to determine the collector current of the current-source transistor, Q_9. The current in the compensated bias divider for Q_9 is

$$I_{C10} = \frac{V^- - 2V_{BE}}{R_6 + R_7} \tag{A.5}$$

The collector current of Q_9 will be

$$I_{C9} = \frac{R_7}{R_8} I_{C10}$$

or

$$I_{C9} = \frac{R_7}{R_8} \left[\frac{V^- - 2V_{BE}}{R_6 + R_7} \right] \tag{A.6}$$

Equation (A.4) now becomes

$$V_{OT} = V_{BE} + \frac{R_1 R_7}{2R_8} \left[\frac{V^- - 2V_{BE}}{R_6 + R_7} \right] \tag{A.7}$$

It is significant that this equation is independent of the positive supply voltage and dependent on resistor ratios, not absolute values. Using the values in Fig. 1,

$$V_{OT} = 0.7V_{BE} + 0.16\,V^- \tag{A.8}$$

which gives a nominal output voltage of 1.4 V with V^- = 6 V and zero input voltage. This is a good choice since the threshold voltage of standard logic circuits is between 0.7 V and 1.7 V. Actually, the exact output voltage is only a secondary consideration since the voltage gain of the comparator is quite high (1,500) so the difference between a 1.4 V and a 0.7 V threshold is only about 0.5 mV at the input.

It can be seen from Eq. (A.8) that the output offset voltage is dependent on the negative supply voltage. However, from the differential of Eq. (A.8),

$$\Delta V_{OT} = 0.16 \quad V^- \tag{A.9}$$

It is evident that a ten-percent change in V^- would give an offset change of 100 μV with a gain of 1,500. The sensitivity of offset to production variations of V_{BE} in Eq. (A.8) is in the order of 20 μV, which is totally negligible.

The above analysis has assumed that all resistors are perfectly matched in ratio. In a practical microcircuit, some mismatches are to be expected. Table A-1 shows the effect of a ten-percent change in individual resistor values on the input offset voltage. It can be seen that the matching of R_1 with R_2 is by far the most significant, giving a 2.5 mV offset for a ten-percent mismatch. However, matches of about two percent, which would give a 0.5 mV offset, are normally obtained in an integrated circuit. Therefore, the mismatching normally seen does not cause significant unbalance. Similarly, it can be shown that the current-gain mismatches usually obtained do not greatly affect offset, except in the input stage where the offset current is determined by the current-gain match.

TABLE A-1

Change in input-referred offset voltage for a 10% decrease in individual resistor values

Resistor	Nominal Value (Ω)	Change in Offset Voltage
R_1	750	+2.4
R_2	750	-2.4
R_4	3900	-0.24
R_5	3900	+0.04
R_6	1600	+0.05
R_7	73	-0.05
R_8	100	+0.05

Finally, the effect of temperature on the output offset voltage (V_{OT}) might be considered. From Eqs. (A.7) and (A.8) it can be seen that the only temperature-sensitive parameter is V_{BE}, since resistors hold their initial room-temperature ratios exceedingly well over a wide temperature range. However, it should be noted that this temperature sensitivity is in the right direction to help compensate for the temperature sensitivity of threshold voltage in logic circuits. Since the temperature variations of logic threshold voltage do not have a significant effect on offset, this is not too important; but at least the temperature sensitivity indicated by Eq. (A.8) improves rather than degrades the performance of the comparator.

The next step in the analysis is to obtain an expression for the voltage gain so that the factors influencing this parameter can be determined. In the analysis, the output conductance of the transistors will be neglected and they will be considered to be unilateral. This does not introduce any appreciable error when double-diffused silicon transistors are used at relatively low voltages as they are here. The terms employed to electrically describe the transistors are the AC current gain and the idealized transconductance obtained by differentiating the expression:

$$I_C = I_S \exp. \frac{q V_{BE}}{kT} \tag{A.10}$$

which gives

$$\frac{\partial I_C}{\partial V_{BE}} = \frac{q I_C}{kT} \tag{A.11}$$

where I_C is the DC collector current, q is the charge of an electron, k is Boltzmann's constant, and T is the absolute temperature. The emitter contact resistance, which is responsible for the difference between the actual and the ideal transconductance, will also be considered. These parameters were chosen to describe the transistors because they are easily related to mask design and processing variables.

With reference to Fig. 1 of the text, the differential voltage gain of the input stage is

$$A_{V1} = \frac{R_2}{\frac{kT}{q I_{C1}} + R_{E1}} \tag{A.12}$$

where R_{E1} is the emitter contact resistance of Q_1.

The voltage gain of the second stage amplifier (Q_4) is likewise

$$A_{V2} = \frac{R_5}{\frac{kT}{q I_{C4}} + R_{E4}} \tag{A.13}$$

The second-stage configuration delivers the full differential gain of the input stage to the second-stage amplifier, so the overall gain will be the product of A_{V1} and A_{V2}. However, the second stage does load the input stage to some degree. The input resistance of the second stage is

$$R_{IN4} = \left[\frac{kT}{q I_{C4}} + R_{E4}\right] h_{fe} \tag{A.14}$$

Hence, the overall gain is

$$A_{VO} = A_{V1} A_{V2} \frac{R_{IN4}}{R_2 + R_{IN4}}$$

$$= \frac{R_2 R_5}{\left[\frac{kT}{qI_{C1}} + R_{E1}\right]\left[\frac{R_2}{h_{fe}} + \frac{kT}{qI_{C4}} + R_{E4}\right]} \qquad (A.15)$$

The input-stage collector current is one-half the current-source current, I_{C9}, given by Eq. (A.6) while the second-stage collector current, I_{C4}, is given by Eq. (A.2).

The sensitivity of the voltage gain to transistor current gains can be estimated by assuming typical values for other variables and plotting gain as a function of h_{fe}. This is done in Fig. A-1. The figure shows that the gain is not greatly affected by h_{fe} variations as long as h_{fe} is above a minimum value. It is also interesting that the gain given by Eq. (A.15) is dependent only on resistor ratios if $R_E << \frac{kT}{qI_C}$ (which is certainly true for acceptable transistors).

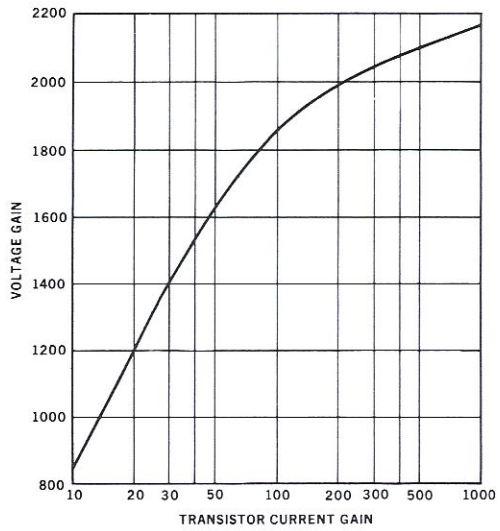


FIG. A-1 Calculated voltage gain as a function current gain of transistor.

An exact analysis of the temperature dependence of gain is quite cumbersome; however, a considerable insight into the functioning of the device can be obtained by looking at the effect of temperature on the individual terms in Eq. (A.15). To start, the variation in resistance values can be neglected since, to a first order approximation, the gain depends only on resistor ratios. The factors that do cause a significant temperature variation of gain are the current gain, which has a positive temperature coefficient, and the transconductance terms, which have a negative temperature coefficient. For moderate current gains, the transconductance terms dominate, giving a negative temperature coefficient of gain as shown in Fig. A-2. With low current gains, the temperature coefficient could be positive because of the dominance of the current-gain term. In this case, the temperature coefficient of gain would be positive at low temperatures where the current gain is low but negative at high temperatures where the current gain is higher.

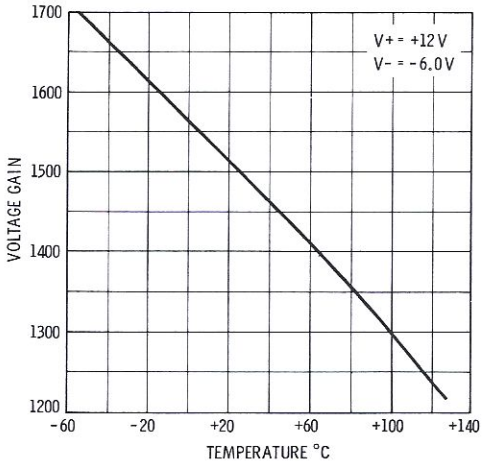


FIG. A-2 Plot of voltage gain as a function of ambient temperature.

Using Eq. (A.15) the change in gain with changes in positive supply voltage can be determined:

$$\frac{\partial A_V}{\partial V^+} = \frac{R_2 R_5 \frac{kT}{qI_{C4}^2} \frac{\partial I_{C4}}{\partial V^+}}{\left[\frac{kT}{qI_{C1}} + R_{E1}\right]\left[\frac{R_2}{h_{fe}} + \frac{kT}{qI_{C4}} + R_{E4}\right]^2} \qquad (A.16)$$

Substituting Eq. (A.15),

$$\frac{\partial A_V}{\partial V^+} = \frac{A_{VO} \frac{kT}{qI_{C4}^2} \frac{\partial I_{C4}}{\partial V^+}}{\frac{R_2}{h_{fe}} + \frac{kT}{qI_{C4}} + R_{E4}} \qquad (A.17)$$

From Eq. (A.2),

$$\frac{\partial I_{C4}}{\partial V^+} = \frac{1}{R_5}$$

and Eq. (A.17) becomes

$$\frac{\partial A_V}{\partial V^+} = \frac{A_{VO}}{\left(V^+ - V_Z - V_{BE} - V_{OT}\right)} \cdot \frac{\frac{kT}{qI_{C4}}}{\left(\frac{kT}{qI_{C4}} + \frac{R_2}{h_{fe}} + R_{E4}\right)} \qquad (A.18)$$

where Eq. (A.2) has been substituted for one of the I_{C4} terms. The second factor in Eq. (A.18) is the ratio of the actual second stage gain to the idealized transconductance-limited gain and has a value less than one (typically 0.6 but less for low-gain devices). Hence,

$$\frac{\partial A_V}{\partial V^+} < \frac{A_{VO}}{V^+ - V_Z - V_{BE} - V_{OT}} \qquad (A.19)$$

Similarly, the change in gain with changes in negative supply voltage can be determined:

$$\frac{\partial A_V}{\partial V^-} = \frac{R_2 R_5 \frac{kT}{qI_{C1}^2} \frac{\partial I_{C1}}{\partial V^-}}{\left[\frac{kT}{qI_{C1}} + R_{E1}\right]^2 \left[\frac{R_2}{h_{fe}} + \frac{kT}{qI_{C4}} + R_{E4}\right]} \qquad (A.20)$$

Where Eq. (A.15) is substituted,

$$\frac{\partial A_V}{\partial V^-} = \frac{A_{VO} \frac{kT}{qI_{C1}^2} \frac{\partial I_{C1}}{\partial V^-}}{\frac{kT}{qI_{C1}} + R_{E1}} \qquad (A.21)$$

Taking $I_{C1} = \frac{I_{C9}}{2}$, where I_{C9} is given by Eq. (A.6),

$$\frac{\partial I_{C1}}{\partial V^-} = \frac{R_7}{2R_8(R_6 + R_7)} \qquad (A.22)$$

Hence,

$$\frac{\partial A_V}{\partial V^-} = \frac{A_{VO}}{V^- - 2V_{BE}} \cdot \frac{\frac{kT}{qI_{C1}}}{\frac{kT}{qI_{C1}} + R_{E1}} \qquad (A.23)$$

where one of the I_{C1} terms has been replaced by $\frac{I_{C9}}{2}$, given by Eq. (A.6). The second term of Eq. (A.23) is, like that of Eq. (A.18), the ratio of the actual input stage gain to the idealized gain. Therefore,

$$\frac{\partial A_V}{\partial V^-} < \frac{A_{VO}}{V^- - 2V_{BE}} \qquad (A.24)$$

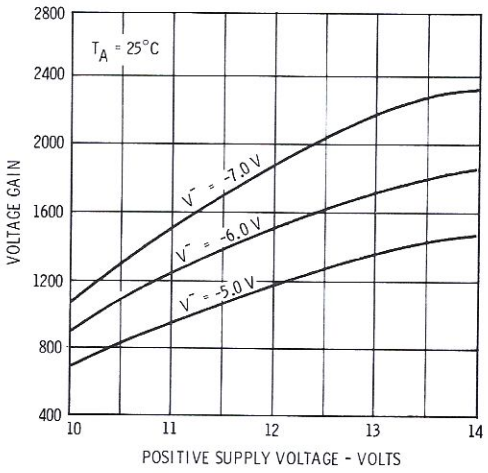


FIG. A-3 Variation of voltage gain with changes in supply voltage.

Equations (A.18) and (A.24) give the maximum gain changes which can be expected for a change in supply voltages. From the derivation of these equations, it can be seen that the decrease in gain for a decrease in supply voltages will be least for the lowest gain devices, which is good since it is only desired to maintain a minimum gain with a comparator. Figure (A-3) shows the variations in gain with supply voltages measured on a typical device.

APPENDIX B

TEST CIRCUITS

This appendix describes test methods that can be used to measure the parameters required to guarantee proper operation of the comparators. The test circuits given are for the μA710, but apply equally well to each half of the μA711 dual comparator, provided the inputs and strobe of the unused half are returned to ground.

Input offset voltage and input offset current can be measured over the entire input voltage using the circuit in Fig. B-1. A μA709 operational amplifier is connected in a feedback loop around the device being tested. The μA709 forces the comparator output to the logic threshold voltage (determined by R_8 and R_9) by adjusting the input voltage to be equal to the offset. Hence, the output voltage of the μA709 is equal to the offset voltage multiplied by the ratio of the precision feedback resistors, R_1 and R_2. This gives a convenient high-level point for measuring offset.

The ±5 V triangular sweep drives the comparator over its specified input voltage range, while the μA709 continuously balances the offset. Hence, if the sweep is used to drive the horizontal amplifier of an oscilloscope and the output of the μA709 drives the vertical amplifier, a display of input offset voltage as a function of input common-mode

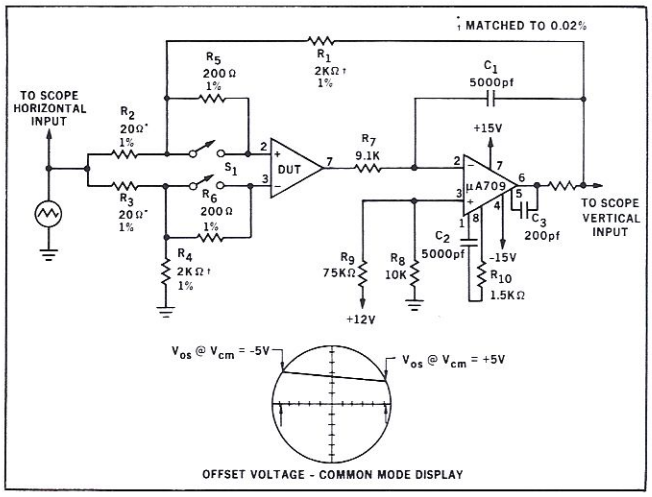


FIG. B-1 Circuit for measuring input offset voltage, input offset current, and common-mode range.

voltage is obtained. The switch, S_1, changes the input source resistance from 20 Ω to 200 Ω, so the offset over the specified range of source resistances can be checked by opening and closing the switch. The offset current is measured from the change in offset voltage when the source resistances are increased.

The resistor pairs (R_1, R_4 and R_2, R_3) must be very closely matched or an erroneous common-mode display will be obtained. In addition, stray capacitances must be kept at a minimum or objectionable hysteresis on the display will result.

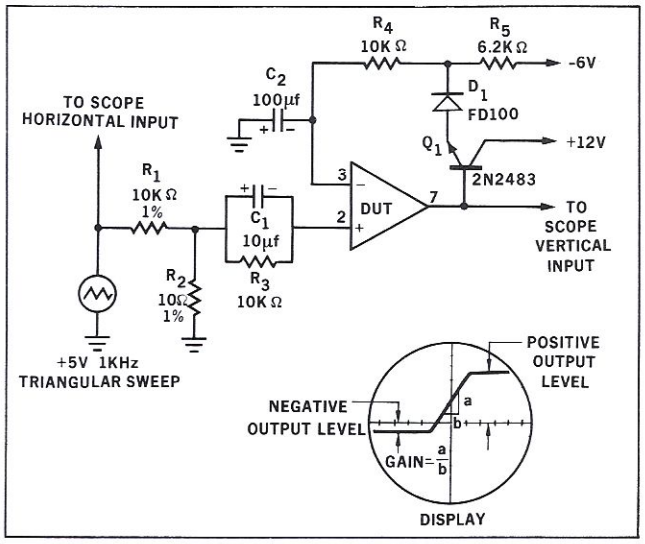


FIG. B-2 Circuit for displaying voltage transfer characteristic.

The voltage transfer characteristic gives much useful information about the operation of the comparator. This is a curve of the input-output characteristics of the circuit over its full dynamic range; gain, positive output level, and negative output level can be determined from a single scope trace. A circuit that can be used to display this function is shown in Fig. B-2. DC feedback stabilizes the operating point of the comparator, with the base-emitter voltage of Q_1 and the forward voltage of D_1 holding the output approximately at the logic threshold level. Capacitor C_2 removes the feedback at the frequency of measurement. The input is driven with the triangular sweep through a resistive divider (R_1 and R_2), which eliminates the need for a high-sensitivity horizontal amplifier on the scope. Typical transfer functions for the μA710 and μA711 are given in Figs. 4 and 5 of the text.

The input bias current is easily measured in the circuit of Fig. B-3. This current is the average of the two input currents, so a resistive divider is used to give a direct reading.

Figure B-4 gives a circuit for measuring loaded, positive output level, strobe current, sink current, and power con-

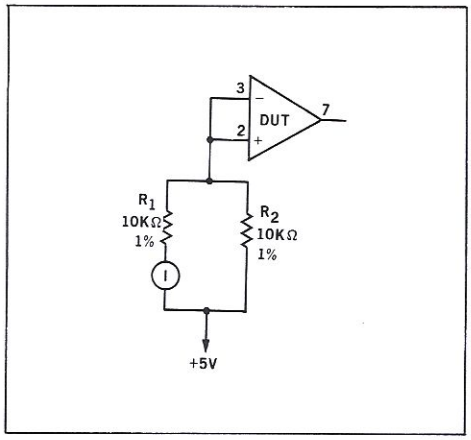


FIG. B-3 Circuit for measuring input bias current.

sumption. A resistive divider at the input provides an input voltage sufficient to drive the comparator to full saturation in either direction. Positive output swing under load is measured with the switch in position 1, and with a 5 KΩ load

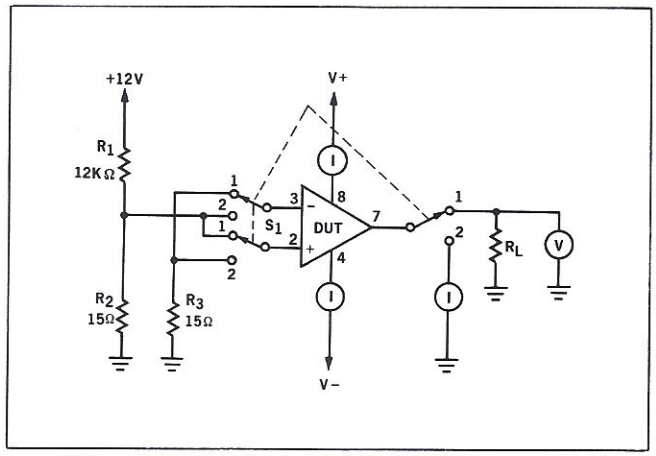


FIG. B-4 Circuit for measuring positive output level, strobe current, sink current, and power consumption.

resistance for the μA710 and a 500 Ω load for the μA711. The strobe current of the μA711 is measured with the switch in this position by connecting the strobe terminal to ground through a current meter. Switch position 2 drives the output to the zero state, which is the condition of maximum power dissipation. Power consumption is computed from the measured positive and negative power supply currents, and sink current is measured directly.

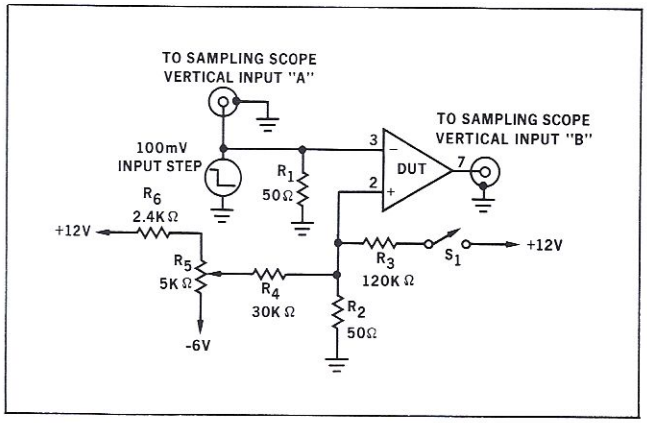


FIG. B-5 Circuit for measuring response time.

The response time of the comparator can be measured with the circuit of Fig. B-5. With S_1 open and the input step at zero, R_5 is adjusted to put the output at the logic threshold voltage. The 100 mV step is then applied and S_1 closed to provide the 5 mV overdrive. The response time is measured from the time the step is applied to the point where the output passes through the logic threshold voltage. Curves of response versus overdrive are given in Fig. 6 of the text.

A simple, self-contained tester that can make relatively complete and rapid tests for use in the laboratory or for incoming inspection is described in Ref. 2.